

Freeform Search

Database:	US Pre-Grant Publication Full-Text Database
	US Patents Full-Text Database
	US OCR Full-Text Database
	EPO Abstracts Database
	JPO Abstracts Database
	Derwent World Patents Index
	IBM Technical Disclosure Bulletins

Term:	L2 and (((predetermin\$3 or pre-determin\$3 or	
	specific\$4) adj (slot\$1 or cycle)) with	
	(access\$3 or read\$3 or writ\$3 or load\$3 or	

Display:	<input type="text" value="10"/>	Documents in Display Format:	<input type="text" value="TI"/>	Starting with Number	<input type="text" value="1"/>
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Generate: ☐ Hit List ☒ Hit Count ☐ Side by Side ☐ Image

Search History

DATE: Monday, March 29, 2004 [Printable Copy](#) [Create Case](#)

<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
side by side			
DB=USPT; PLUR=YES; OP=OR			
<u>L3</u>	L2 and (((predetermin\$3 or pre-determin\$3 or specific\$4) adj (slot\$1 or cycle)) with (access\$3 or read\$3 or writ\$3 or load\$3 or stor\$3))	24	<u>L3</u>
<u>L2</u>	711/104,105,106.ccls. or 711/167,169.ccls. or 365/222,189.01,200,193.ccls. (711/104,105,106.ccls. or 711/167,169.ccls. or 365/222,189.01,200,193.ccls. and	6537	<u>L2</u>
<u>L1</u>	((predetermin\$3 or pre-determin\$3 or specific\$4) adj (slot\$1 or cycle)) with (access\$3 or read\$3 or writ\$3 or load\$3 or stor\$3)))	0	<u>L1</u>

END OF SEARCH HISTORY

Freeform Search

Database:	US Pre-Grant Publication Full-Text Database US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins
Term:	L7 and ((slot\$1 or cycle) with (access\$3 or read\$3 or writ\$3 or load\$3 or stor\$3))
Display:	<input type="text" value="10"/> Documents in Display Format: <input type="text" value="TI"/> Starting with Number <input type="text" value="1"/>
Generate: <input type="radio"/> Hit List <input checked="" type="radio"/> Hit Count <input type="radio"/> Side by Side <input type="radio"/> Image	

Search

Clear

Interrupt

Search History

DATE: Monday, March 29, 2004 [Printable Copy](#) [Create Case](#)

<u>Set Name</u> side by side	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L8</u>	L7 and ((slot\$1 or cycle) with (access\$3 or read\$3 or writ\$3 or load\$3 or stor\$3))	67	<u>L8</u>
<u>L7</u>	L4 and ((predetermin\$3 or pre-determin\$3 or specific\$4) adj (slot\$1 or cycle))	81	<u>L7</u>
<u>L6</u>	L4 and ((predetermin\$3 or pre-determin\$3 or specific\$4) adj3 (slot\$1 or cycle))	299	<u>L6</u>
<u>L5</u>	L4 and ((predetermin\$3 or pre-determin\$3 or specific\$4) with (slot\$1 or cycle))	920	<u>L5</u>
<u>L4</u>	l1 or l2 or L3	6537	<u>L4</u>
<u>L3</u>	365/222,189.01,200,193.ccls.	4818	<u>L3</u>
<u>L2</u>	711/167,169.ccls.	1179	<u>L2</u>
<u>L1</u>	711/104,105,106.ccls.	920	<u>L1</u>

END OF SEARCH HISTORY

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First Hit Fwd Refs

Generate Collection

L3: Entry 21 of 24

File: USPT

Sep 1, 1992

DOCUMENT-IDENTIFIER: US 5144581 A

TITLE: Apparatus including atomic probes utilizing tunnel current to read, write and erase erase data

Current US Cross Reference Classification (6):
365/189.01

CLAIMS:

2. The apparatus according to claim 1, wherein said arithmetic operation is sampling of information, and said control means comprises

writing means for controlling said scanning means and said information writing means to write said information from said information generator in the small capacity recording region of said recording medium at a first timing of a predetermined cycle, and

reading means for controlling said scanning means and said information reading means to read out said information from the small capacity recording region of said recording medium at a second timing of the predetermined cycle.

First Hit Fwd Refs

Generate Collection

L4: Entry 26 of 30

File: USPT

Feb 21, 1989

DOCUMENT-IDENTIFIER: US 4807289 A

TITLE: Apparatus for recording and reproducing human speech by its analysis and synthesis

Abstract Text (1):

A speech analysis and synthesis device comprises analyzing and synthesizing means for analyzing human speech to produce analyzed data and for synthesizing human speech on the basis of the analyzed data, a dynamic RAM for memorizing the analyzed data, a refresh address counter for outputting a refresh address sequentially varying every a predetermined refresh cycle for designating a memory location of the dynamic RAM, an access address counter for outputting an access address indicative of a memory location where the analyzed data is accessed, and refresh-access means for effecting a refresh operation of a memory cell assigned to the refresh address every the predetermined refresh cycle and for providing an access to a memory cell assigned to the access address in synchronism with the predetermined refresh cycle during non-refresh cycle. The speech analysis and synthesis device enables connection of the dynamic RAM without provision of complicated peripheral circuits.

Brief Summary Text (7):

To achieve this object, there is provided an apparatus for analyzing and synthesizing human speech comprising: means for analyzing human speech to produce analyzed data and for synthesizing human speech on the basis of said analyzed data; a dynamic RAM for memorizing said analyzed data; a refresh address counter for outputting a refresh address sequentially varying every predetermined refresh cycle, said refresh address indicating a location of a memory cell to be refreshed in said dynamic RAM; an access address counter for outputting an access address indicative of a location of a memory cell where said analyzed data in said dynamic RAM is accessed; and means for effecting a refresh operation of a memory cell assigned to said refresh address every said predetermined refresh cycle and for providing an access to a memory cell assigned to said access address in synchronism with said predetermined refresh cycle for a time period during which a refresh operation is not effected.

Current US Cross Reference Classification (1):365/222

First Hit Fwd Refs

Generate Collection

L4: Entry 21 of 30

File: USPT

Apr 4, 1995

DOCUMENT-IDENTIFIER: US 5404335 A

TITLE: Dynamic type semiconductor memory device operable in a self-refreshing mode

Brief Summary Text (43):

In the self-refreshing mode, the refreshing address counter 120 generates the refreshing address. For the periodical refreshing of the memory cells in each row in the memory cell array in the DRAM, it is necessary to operate the refreshing address counter correctly and to generate the refreshing address periodically. If refreshing address counter 120 is a ten-bit counter, the counter is required to generate the same refreshing address every 1024 cycles.

Current US Original Classification (1):365/222Current US Cross Reference Classification (1):365/193